Amendments to the Specification:

Please replace the two paragraphs beginning at page 34 line 4 and page 34 line 7 which comprise the Abstract with the following amended paragraph:

~~The current invention provides a Fourier transform processor with a wide range of applications including communications, signal processing, medical and other imaging, seismic analysis, radar and other military applications, pattern recognition, signal processing etc.~~ ~~The~~ A Fourier transform processor ~~utilizes~~ utilizing discrete circuits each of which is configurable for processing a wide range of sample sizes. A single pipeline supports multiplexed bi-directional transformations between for example the time and frequency domains. In an embodiment of the invention the Fourier Transform processor may be implemented as part of a digital signal processor (DSP). In this embodiment the DSP may implement both the discrete Fourier transform (DFT) and inverse discrete Fourier transform (IDFT) across a wide range of sample sizes and X-DSL protocols. Multiple channels, each with varying ones of the X-DSL protocols can be handled in the same session.

a1

Please replace the paragraph beginning at page 1 line 7 which comprises the Cross Reference to Related Application with the following amended paragraph:

This application claims the benefit of prior filed ~~co-pending~~ Provisional Application No. 60/161,744 entitled "BURST MODE ENGINE" ~~and~~ filed on October 26, 1999 ~~(Attorney Docket # VELCP003P)~~; and ~~co-pending~~ Provisional Application No. 60/179,862 entitled "DMT ENGINE" filed on February 2, 2000 ~~(Attorney Docket# VELCP010P)~~. Each of the above-cited applications is incorporated herein by reference in its entirety.

a2

Please replace the paragraph beginning at page 1 line 27 with the following amended paragraph:

Digital Subscriber Lines (DSL) technology and improvements thereon including: splitterless asymmetric digital subscriber lines (G.Lite), Asymmetric Digital Subscriber Line

a3

(ADSL), very high data digital subscriber line (VDSL), symmetric digital subscriber line(SDSL), medium-speed digital subscriber line (MDSL), rate adaptive digital subscriber line (RADSL), high-bit-rate digital subscriber line(HDSL), etc. all of which are broadly identified as X-DSL have been developed to increase the effective bandwidth of existing subscriber line connections, without requiring the installation of new fiber optic cable. An X-DSL modem operates at frequencies higher than the voice band frequencies, thus an X-DSL modem may operate simultaneously with a voice band modem or a telephone conversation.

a3

Please replace the paragraph beginning at page 11 line 22 with the following amended paragraph:

On the upstream packet path, the AFE PAD includes a first-in-first-out (FIFO) buffer 400 where upstream packets from the AFEs are stored and a cyclic prefix remover 404. After removal of the cyclic prefix each packet is then passed to the DFT mapper 424. The DFT mapper is coupled to the input memory portion of the FTE via a multiplexer 420. The mapper handles writing of each sample set from a packet into the input memory in the appropriate order. The mapper may also handle such additional functions as time domain equalization (TEQ) filtering which is a digital process designed to normalize the impact of differences in channel response. The filter may be implemented as ~~an~~ a finite impulse response(FIR) filter. The input memory comprises two portions 416 and 418. Multiplexer 420 provides access to these memories. While one sample set, e.g. time or frequency domain data, is being written from the upstream or downstream data paths into one of the memories the contents of the other of the memories are written into the row and column component 412 of the FTE 322. Once the DFT is completed by the row and column component the frequency domain coefficients generated thereby are stored in either of portions 408-410 of the output memory of the FTE. These coefficients correspond with each of the DMT subcarriers. A multiplexer 408 handles the coupling of the output memory to either the next component of the upstream path, i.e. the deframer-decoder 332 or of the downstream path. Next on the upstream path, the device packet with header and data portions and optional control portion is passed to the remaining components of the upstream path. These include the gain scalar and optional forward error correction (FEQ) 424, the decoder 426, the tone re-orderer 428 and the deframer 432.

a4